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Third Semester B.E. Degree Examination, Jan./Feb. 2023 Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Explain the construction and working principle of LED. (05 Marks)
- b. List the types of transistor biasing. Explain Fixed Bias Circuit with necessary analysis. (06 Marks)
- c. Explain the operation of astable multivibrator using IC555 and derive the expression for time period, frequency and duty cycle. (09 Marks)

OR

- 2 a. Explain the operation of peak detector circuit with neat diagram. (05 Marks)
- b. List and explain the performance parameters of regulated power supply. (06 Marks)
- c. Explain the 3 bit flush type ADC with necessary circuit and truth table. (09 Marks)

Module-2

- 3 a. Find the minimum sum of products using K-map and identify prime implicants.
 $f(a, b, c, d) = \sum m(0, 2, 6, 10, 11, 12, 13) + d(3, 4, 5, 14, 15)$ (06 Marks)
- b. Find the minimum SOP and POS using K-map
 $f(a, b, c, d) = \sum m(6, 7, 9, 10, 13) + d(1, 4, 5, 11)$ (08 Marks)
- c. List the steps for Petrick's method. (06 Marks)

OR

- 4 a. Find all the prime implicants using Quine Mc Cluskey method. Verify the result using K-map.
 $f(w, x, y, z) = \sum m(7, 9, 12, 13, 14, 15) + d(4, 11)$ (12 Marks)
- b. Using Prime implication chart, find all the minimum SOP of the function using Quine McCluskey method.
 $f(a, b, c, d) = \sum m(0, 1, 2, 3, 10, 11, 12, 13, 14, 15)$ (08 Marks)

Module-3

- 5 a. Realize the function using only two input NAND gate and inverters.
 $f_1 = \sum m(0, 2, 3, 4, 5)$, $f_2 = \sum m(0, 2, 3, 4, 7)$, $f_3 = \sum m(1, 2, 6, 7)$ (06 Marks)
- b. Draw the timing diagram of the circuit. Assume propagation delay of each gate is 20 ns. (05 Marks)

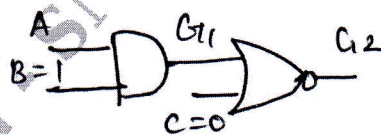


Fig. Q5 (b) - (i)

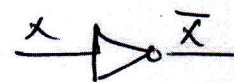


Fig. Q5 (b) - (ii)

- c. List the types of hazards. Explain how static 1 hazard can be detected and removed with suitable example. (09 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

OR

- 6 a. Write short notes on three state buffers. (06 Marks)
 b. Design 7-segment decoder using PLA. (06 Marks)
 c. Construct 8 : 1 mux using only 2 : 1 mux. (08 Marks)

Module-4

- 7 a. Given that $A = "00101101"$ and $B = "10011"$. Determine the value of F
 $F \leftarrow \text{not } B \& "0111" \text{ or } A \& "1" \text{ and } "1" \& A$ (04 Marks)
 b. Write the complete VHDL code for 4 bit binary adder. (08 Marks)
 c. Explain how the VHDL code can be compiled simulated and synthesized with example. (08 Marks)

OR

- 8 a. Explain T Flip Flop with truth table. (07 Marks)
 b. Explain Master-Slave JK flip flop with neat diagram. (08 Marks)
 c. Write short notes on switch debouncing with an SR Latch. (05 Marks)

Module-5

- 9 a. Explain 8 bit serial in serial out shift register. (10 Marks)
 b. Explain n bit parallel adder with accumulator. (10 Marks)

OR

- 10 a. Design and explain mod 8 synchronous counter using JK flip flop. (10 Marks)
 b. Explain how moore transition and states can be constructed with examples. (10 Marks)
